Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	3

Complete if Known	
Application Number	10/612,775
Filing Date	July 2, 2003
First Named Inventor	Kuo-Hsing Cheng
Art Unit	2825
Examiner Name	Thompson, Annette M
Attorney Docket Number	4728P042D

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
CAA		SHELDON B. AKERS, "clustering Techniques For Vlsi", CH1681-6/82/0000-0472, 1982 IEEE (pp. 472-476)	
CAA		CHARLES J. ALPERT, et al., "Multilevel Circuit Partitioning", UCLA Computer Science Dept., L.A., CA., (Paper 32.5; pp. 530-533)	
CAA		CHARLES J. ALPERT, et al., "Spectral Partitioning: The More eigenvectors, The Better", UCLA Computer Science Department, L.A., CA., 32nd ACM/IEEE Design Automation Conference (6 pages)	
CAA		JASON CONG, et al., "Large Scale Circuit Partitioning With Loose/Stable Net Removal And Signal Flow Based Clustering", 1092-3152/97, 1997 IEEE (pp. 441-446)	
CAA		JASON CHONG, et al., "Multiway Partitioning with Pairwise Movement", UCLA Dept. of Computer Science, L.A., CA (pp. 512-516)	
CAA		SHANTANU DUTT, et al., "A Probability-Based Approach to VLSI Circuit Partitioning", Dept. of Electrical Engineering, Univ. of Minnesota, Minneapolis, MN (Paper 6.4; pp. 100-104)	
CAA		SHANTANU DUTT, "New Faster Kernighan-Lin-Type Graph-Partitioning Algorithms", Dept. of Electrical Engineering, Univ. of Minnesota, Minneapolis, MN., 1063-6757/93, 1993 IEEE (pp. 370-377)	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/612,775
				Filing Date	July 2, 2003
(use as many sheets as necessary)				First Named Inventor	Kuo-Hsing Cheng
				Art Unit	2825
				Examiner Name	Thompson, Annette M
Sheet	2	of	3	Attorney Docket Number	4728P042D

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
CM		C.M. FIDUCCIA et al., "A LINEAR-TIME HEURISTIC FOR IMPROVING NETWORK PARTITIONS", 19TH Design Automation Conference, 0420-0098/82/0000/0175, 1982 IEEE, (Paper 13.1; pp. 175-181)	
CM		JORN GARBERS, et al., "Finding Clusters In VLSI Circuits", Research Institute of Discrete Mathematics; CH2924-9/90/0000/0520, 1990 IEEE (pp. 520-523)	
CM		M.R. GAREY, et al., "Computers and Intractability", A2 Network Design (pp. 209-219)	
CM		MICHAEL R. GAREY, et al., "Computers and Intractability" A guide to the Theory of NP-Completeness, Bell Laboratories (2 pages)	
CM		LARS HAGEN, et al., "Fast Spectral Methods For Ratio Cut Partitioning and Clustering", UCLA Dept. of Computer Science, L.A., CA. CH3026-2/91/0000/0010, 1991 IEEE (pp. 10-13)	
CM		MICHAEL A.B. JACKSON, et al., "A Fast Algorithm For Performance-Driven Placement", Electronics Research Lab, Univ. of Calif., Berkeley, CA, CH2924-9/90/0000/0328, 1990 IEEE, (pp. 328-331)	
CM		B.W. KERNIGHAN, et al., "An Efficient Heuristic Procedure For Partitioning Graphs", Manuscript received September 30, 1969, (pp. 291-307)	

Examiner Signature	Annette E. Thompson	Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/612,775
				Filing Date	July 2, 2003
(use as many sheets as necessary)				First Named Inventor	Kuo-Hsing Cheng
				Art Unit	2825
				Examiner Name	Thompson, Annette M
Sheet	3	**of**	3	Attorney Docket Number	4728P042D

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
CAT		DONALD E. KNUTH, "The Art of Computer Programming", Vol. 3/Sorting and Searching, Addison-Wesley Publ. Company, This book is in the Addison-Wesley Series In Computer Science and Info. Processing, (6 pages)	
CAT		BALAKRISHNAN KRISHNAMURTHY, "An Improved Min-Cut Algorithm For Partitioning VLSI Networks", IEEE Transactions on Computers, Vol. C-33, No. 5, May 1984, (pp. 438-446)	
CAT		YOUSSEF G. SAAB, "A Fast and Robust Network Bisection Algorithm", IEEE Transactions on Computers, Vol. 44, No. 7, July 1995, (pp. 903-913)	
CAT		CARL SECHEN, "VLSI Placement and Global Routing Using Simulated Annealing, Book Series: The Kluwer Int'l Series In Engineering and Computer Science: Vol. 54 (1 page)	
CAT		NAVEED A. SHERWANI, "Algorithms For VLSI Physical Design Automation" Third Edition, Kluwer Academic Publishers, (3 pages)	
CAT		CHUNG-KUAN CHENG, "An Improved Two-Way Partitioning Algorithm With Stable Performance", IEEE Transactions on Computer-Aided Design, Vol. 10, No. 12, December 1991, (pp. 1502-1511)	
CAT		YEN-CHUEN WEI, et al., "Towards Efficient Hierarchical Designs By Ratio Cut Partitioning", Computer Science and Engineering Dept., Univ. of Calif., San Diego, La Jolla, CA. CH2805-0/89/0000/0298, 1989 IEEE, (pp. 298-301)	

Examiner Signature		Date Considered	

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

[1]Applicant's unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 08/11/2003.
Send To: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450